What is claimed is:

1. A circuit comprising:

a shift register connected to an input node, the shift register including a plurality of register cells;

a select circuit connected to a subset of the plurality of register cells through a number of select lines, the select circuit including an output node; and

a controller connected to the select circuit and the register cells to configure the register cells to select only one of the select lines to be a part of a conductive path connected between the input node and the output node.

2. The integrated circuit of claim 1, wherein the number of register cells equals 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit.

3. The integrated circuit of claim 1, wherein the number of select lines equals a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit.

4. The integrated circuit of claim 1, wherein the select circuit includes:

an encoder including a plurality of inputs connected to the select lines, and a plurality of encoder outputs; and

a multiplexer including a plurality of inputs connected to the select lines, a plurality of multiplexer inputs connected to the encoder outputs, and a multiplexer output connected to the output node of the select circuit such that the multiplexer is set to pass only data bits to the multiplexer output node from a select line that is configured by the controller.

5. The integrated circuit of claim 1 further comprising a logic circuit connected to the register cells to perform a logic function on data held in the register cells.

6. The integrated circuit of claim 5, wherein the logic circuit includes:

a calculation unit to perform a logic function on a plurality of bits;

a plurality of memory units to store results from the logic function;

a counter to count values stored in the memory units; and

a detect logic responsive to the counter to generate a rotation number, the rotation number being used to rotate the data held in the register cells.

7. The integrated circuit of claim 6, wherein the logic function performs an OR function.

8. The integrated circuit of claim 7, wherein the memory units are arranged in rows and columns, wherein the memory units in the same row form a shift register.

9. The integrated circuit of claim 8, wherein the counter includes a plurality of counter memory units, each of the counter memory units being connected to one shift register.

10. An integrated circuit comprising:

a plurality of input nodes to receive a plurality of input bits;

a plurality of output nodes to provide a plurality of output bits;

a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes;

a logic circuit connected to the register circuits to perform a logic function on a plurality of bits held by the register circuits; and

a controller to configure the register circuits based on a result from the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at the input nodes are misaligned by one or more bit time intervals.

11. The integrated circuit of claim 10, wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit.

12. The integrated circuit of claim 11, wherein each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines.

13. The integrated circuit of claim 12, wherein the number of select lines equals a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit.

14. The integrated circuit of claim 13, wherein the logic circuit includes:

a calculation unit to perform a logic function on a plurality of bits;

a plurality of memory units to store results from the logic function;

a counter to count values stored in the memory units; and

a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells.

15. The integrated circuit of claim 10, wherein the logic function performs an OR function.

16. The integrated circuit of claim 14, wherein the memory units are arranged in rows and columns, wherein the memory units in the same row form a shift register.

17. The integrated circuit of claim 14, wherein the counter includes a plurality of counter memory units, each of the counter memory units being connected to one shift register.

18. A system comprising:

a parallel bus including a plurality of bus lines to carry a plurality of bits on each of the bus lines; and

a first integrated circuit including a plurality of register circuits, each of the register circuits being connected to one of the bus lines, and each of the register circuits including,

a shift register connected to an input node, the shift register including a plurality of register cells,

a select circuit connected to a subset of the number of register cells through a number of select lines, the select circuit including an output node, and

a controller connected to the select circuit and the register cells to configure the register cells to select only one of the select lines to be a part of a conductive path connected between the input node and the select circuit output node.

19. The system of claim 18 further comprising a second integrated circuit connected to the parallel bus.

20. The system of claim 19, wherein the parallel bus is formed on a circuit board, and the first and second integrated circuits are located in the circuit board.

21. The system of claim 19 further comprising:

a first circuit board, wherein the parallel bus is formed on the first circuit board and the first integrated circuit is located on the first circuit board; and

a second circuit board, wherein the second integrated circuit is located on the second circuit board, the second circuit board being inserted into a bus slot that connects to the parallel bus.

22. The system of claim 19, wherein the first and second integrated circuits are located on separate circuit boards, and the parallel bus is not formed on the first or second circuit boards.

23. A method of aligning bits on a parallel bus, the method comprising:

receiving at each of a plurality of registers a plurality of training bits transmitted on each of a plurality of bus lines of a parallel bus during an initialization process;

determining an actual number of bit time intervals of misalignment among the plurality of training bits during transmission on the parallel bus lines based on the plurality of training bits; and

configuring the registers based on the actual number of bit time intervals of misalignment to align subsequent functional bits transmitted on each of the bus lines of the parallel bus after the initialization process, in which the subsequent functional bits are misaligned by at least one bit time interval during transmission on the parallel bus.

24. The method of claim 23, wherein receiving a plurality of training bits includes receiving a pattern of bits, the pattern of bits including a bit that represents a first logic value and a plurality of bits that represents a second logic value.

25. The method of claim 23, wherein receiving a plurality of training bits includes receiving a pattern of bits, the pattern of bits including a bit that represents a first logic value and 2M-2 number of bits that represents a second logic value, wherein M is the maximum number of bit time intervals of misalignment that the integrated circuit can tolerate.

26. The method of claim 23, wherein determining an actual number of bit time intervals of misalignment includes:

performing a logic function on each bit position of each of the registers to produce a plurality of resultant bits;

generating an array of bits based on the resultant bits; and

selecting a row of bits from the array of bits.

27. A method of aligning bits on a parallel bus, the method comprising:

loading a plurality of training bits transmitted on each of a plurality of bus lines into each of a plurality of registers;

performing a logic function on the training bits loaded in the registers to produce a plurality of resultant bits;

generating an array of bits based on the resultant bits;

determining a number of rotations based on the array of bits;

rotating the training bits in the plurality of registers based on the number of rotations; and

configuring transmission paths between the plurality of bus lines and a plurality of outputs based on logic values of bits in the registers.

28. The method of claim 27, wherein transmitting a plurality of training bits includes transmitting a pattern of bits, the pattern of bits including a bit that represents a first logic value and a plurality of bits that represents a second logic value.

29. The method of claim 27, wherein transmitting a plurality of training bits includes transmitting a pattern of bits, the pattern of bits including one bit that represents a first logic value and 2M-2 number of bits that represents a second logic value, wherein M is a maximum number of bit time intervals of misalignment that the integrated circuit can tolerate.

30. The method of claim 27, wherein generating an array of bits includes generating a 2M-1 by 2M-1 array of bits, wherein M is a maximum number of bit time intervals of misalignment of the parallel bus.